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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,303	08/10/2001	Peter Rabkin	00939A-085100US	4969

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EXAMINER	
BERRY, RENEE R	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 02/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,303	RABKIN ET AL.	
	Examiner	Art Unit	
	Renee R Berry	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *12-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I is acknowledged.

Claims 12-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent no. 6,071,775 to Choi et al. in view of US patent no. 5,641,696 to Takeuchi.

In regards to claim 1, Choi teaches a method for forming on a silicon substrate a non-volatile memory cell in an array region and a transistor in a region peripheral to the array region, the method comprising: forming a polysilicon gate stack in the array region, and a transistor polysilicon gate in the peripheral region; forming one of LDD and DDD regions in one or both source and drain regions of the transistor, forming a spacer along one or more side-walls of each of the cell gate stack and the transistor gate; forming an oxide layer over the spacers, the cell gate stack, and the transistor

gate; forming a highly doped region in each of said one of the LDD and DDD regions, wherein a lateral distance between an outer edge of the highly doped diffusion region and an outer edge of a corresponding one of LDD and DDD regions is dependent at least on a thickness of the oxide layer, defining a contact hole area over one or both drain and source regions of the memory cell using a masking layer, wherein the contact area abuts or overlaps the polysilicon stack, and performing a contact etch to form a contact hole in the contact hole area, wherein the spacer is substantially resistant to the contact etch at column 7, lines 35-58.

In regards to claim 2, Choi teaches before the oxide layer-forming act, forming a sacrificial layer over the spacers, the cell gate stack, and the transistor gate at column 10, lines 1-9.

In regards to claim 3, Choi teaches the spacer and the sacrificial layer comprised nitride at column 8, lines 15-19.

In regards to claim 4, Choi teaches the contact etch removes the oxide layer and part or all of the sacrificial layer at column 8, lines 59-63.

In regards to claim 5, Choi teaches one of the LDD and DDD regions forming act is carried out after the spacer-forming act but before the oxide layer-forming act at column 7, lines 36-40.

In regards to claim 6, Choi teaches the spacer is insulated from the sidewalls of polysilicon layers in the gate stack at column 10, lines 1-6.

In regards to claim 9, Choi teaches prior to the highly doped region forming act, performing an oxide etch to remove at least portions of the oxide layer over the drain and source regions of the transistor at column 8, lines 59-63.

In regards to claim 10, Choi teaches prior to the spacer forming act, forming a DDD region in the source or drain region of the cell; and after the spacer forming act, forming a highly doped region in the DDD region at column 2, lines 62-67.

However, Choi does not teach all the limitations of the claims.

In regards to claim s 1 and 7, Takeuchi teaches forming an HTO layer over the gate stack to insulate the gate stack from the spacer at column 10, lines 25-38.

In regards to claim 8, Takeuchi teaches forming the source and drain regions of the memory cell after the HTO layer-forming act at column 10, lines 62-67.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Choi to include forming an HTO layer over the gate stack to insulate the gate stack from the spacer and forming the source and drain regions of the memory cell after the HTO layer-forming act, since such a modification would result in the suppression of the short channel effect, as described in column 2, lines 34-40 of TaKeuchi.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US patent no. 6,051,465 to Kato discloses a method for forming on a silicon substrate a non-volatile memory cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

RRB

January 13, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800